P24677

Form PTO-1449 U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. P24677	Serial No. 10/748,242
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant Ryutaro YAMANAKA et al	
	Filing Date December 31, 2003	Group 2133

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	CLASS		S	FILING DATE IF APPROPRIATE
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	09	-148943	06/06/97	JAPAN			X	
	63	-215227	09/07/88	JAPAN			X	
	6-	164423	06/10/94	JAPAN				
		8-84082	09/14/94	JAPAN				
	9-	148943	11/17/95	JAPAN				
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		1 English Language Abstract JP 09-148943.
		2 English Language Abstract JP 63-215227.
		3 UEDA et al., "A 16-bit Digital Signal Processor with Specially Arranged Multiply-Accumulator for Low Power Consumption", IEICE Trans. Electron, Vol. E78-C, No. 12, December 1995.

EXAMINER	DATE CONSIDERED 7/31/06

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	4	H. LOU, "Viterbi Decoder Design for the IS-95 CDMA Forward Link", IEEE 46th Vehicular Technology Conference, No. 2, 1996, pp.1346-1350.
	5	English Language Abstract of JP6-164423.
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	9	English Language Abstract of10-209882.
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